A Software Definable MIMO Testbed: Architecture and Functionality

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***Abstract*- Following the intensive theoretical studies of recently emerged MIMO technology, a variety of performance measures become important to investigate the challenges and trade-offs at various levels throughout MIMO system design process. This paper presents a review of the MIMO testbed recently set up at King's College London. The architecture that distinguishes the testbed as a flexible and reconfigurable system is first preseneted. This includes both the hardware and software aspects, and is followed by a discussion of implementation methods and evaluation of system research capabilities.**

I. INTRODUCTION

Multiple-input-multiple-output (MIMO) has recently emerged as one of the most significant technical breakthrough in modern mobile and fixed wireless communication systems because of the increase it offer in throughput and reliability. While theoretical studies involving stochastic channel models [1] and geometrical channel models [2] have explored the ideal capacity gains of MIMO systems, recent measurement campaign results further demonstrate the benefits of MIMO channels [3-5]. Meanwhile, various transmission schemes over MIMO channels have been proposed to develop practical algorithms with reasonable BER performance/complexity compromise in conjunction with high spectral efficiency. Space-time coding has emerged as special channel coding techniques assisted with MIMO channels to introduce temporal and spatial correlations into transmission and achieve reasonable diversity and coding performance [6].

With MIMO-related theoretical research entering a mature stage, hardware testbeds and platforms have become essential in validating the performance gains over real channels and in the presence of implementation impairments. Most recently, various testbeds are reported in the literatures that focus on various implementation aspects of MIMO systems [7-12]. According to the system architecture, current MIMO testbeds typically fall into three categories: PC-based software-define broadband testbed, DSP-based narrowband testbed and ASIC-FPGA-based high-speed testbed. The system performance, research capability and costs of various testbeds are addressed and compared in [13].

The Centre for Telecommunications Research (CTR) at King's College London (KCL) has recently acquired a MIMO testbed based on two 4X4 MIMO test platforms (STAR Platform from Tait Electronics NZ) [14]. The testbed is based on an architecture that is a hybrid of the three mentioned above: with two 4X4 transceiver platforms connected to a PC server through an Ethernet-based data acquisition interface, and each platform integrates FPGA, DSP and CPU. The platforms operate in the 2.4GHz ISM band with a configurable RF bandwidth of either 3.84MHz or 17MHz; they allow arbitrary modulation formats, space-time codes and MIMO algorithms to be implemented. This paper focuses on the system architecture, implementation method, research capabilities and limitations of this MIMO testbed.

The paper is organized as follows. In Section II, we present the system architecture of the STAR testbed, including both hardware and software architecture. Next, in Section III, we discuss and evaluate the capability and limitations of various implementation methods on the MIMO platform. The current challenges of the platform development are addressed in Section IV. Finally, Section V describes the future work and concludes this paper.

II. SYSTEM ARCHITECTURE

A. System Hardware Architecture

As shown in figure 1, the MIMO testbed consists of three main blocks: User's PCs, PC Server and two Platform Transceivers with unique IP addresses. "FTP interface" and "NFS interface" are Ethernet-based software running on the PC server to create a maximum 10Mbyte/s bandwidth logical connection mainly used for data acquisition. "Web page interface", "RS232 interface" and "Telnet interface" are lower bandwidth logical connections merely used for control and debugging.

It is through the logical connections that different parts interact with others to exchange data and control information. A typical implementation cycle on the MIMO testbed is presented as follows. The control scripts, implementation files or simulation data are generated on user's PCs and sent to the server through the web page interface. The server simply stores them as files in different dedicated directories. The Platform Transceivers are programmed to keep searching those dedicated directories on the server through the Linux NFS interface. If any new instructions are found, they will update themselves automatically by downloading and executing control scripts written in certain formats. Following the control scripts, the

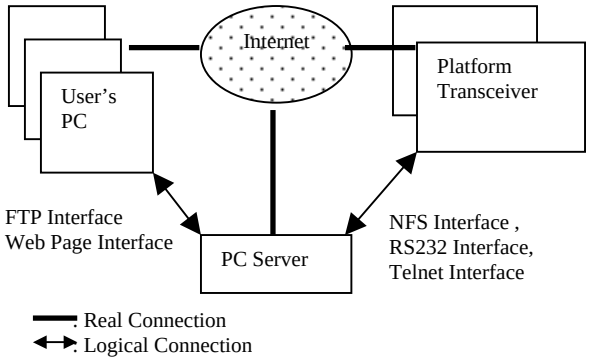

Figure 1: MIMO Testbed System Architecture

platform transceiver is able to be reconfigured, read simulation data form the server, modulate and transmit data into a real world wireless channel, then capture the signal, sample, process and store them back as files into the server. Therefore the received data, which could be either over-sampled digital IF waveforms or demodulated information bit, is available on the server for users to download and analyze.

B. Platform Transceiver Hardware Architecture

Each platform transceiver is a reconfigurable integrated unit capable of providing up to 4 transmit and 4 receive channels by the parallel combination of RF and digital processor sub-systems. The whole platform consists of four sub-units: the digital processor sub-system (digital board), the mixed signal front end (mixed signal board), the RF sub-system (RF transmit and receive board) and the Synth Board [14]. Interfacing details among four sub-units are showed in figure 2.

The digital board is designed for interfacing the outside world and processing baseband signals. By closely interfaced ARM processor (S3C2410X01), FPGA (Altera Stratix EP1S25), and DSP (TMS320C6416GLZ), the digital sub-system can be scaled to provide more processing capability and channels. The ARM processor acts as the control CPU on the digital board. The embedding of the Linux operating system enables all the system control and monitoring functions. The FPGA unit is considered as both the data hub and the main processing resource for low-level, high speed parallel processing. The main role of the DSP unit is to run certain user's algorithms on a higher level or to provide extra signal processing capability when the FPGA resources are unavailable.

On the mixed signal board, four ADCs and DACs (AD9862) operates at a rate of 60 Msample/s providing four parallel 15MHz digital IF interfaces.

The RF boards execute two-step frequency conversions to/from the RF operating frequency within the 2.4GHz to

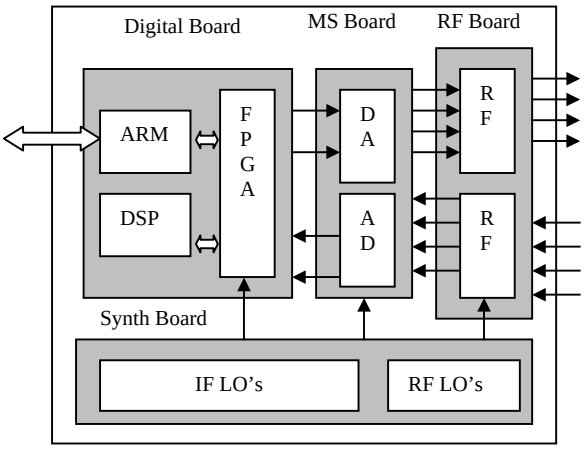

Figure 2: Platform Transceiver Hardware

2.5GHz ISM band, although additional up/down converter stages would allow the operational band to be changed (eg.5GHz). The RF board provides four differential 15MHz IF analog interfaces to the mixed signal board. The transmit up-converter board provides 25dB of gain with a maximum output power of 17dBm. The receive down-converter provides 43dB gain with an input 3rd order intercept of –20dBm. The noise figure of the receiver up to the input to the A/D is 8dB. The IF-stage consists of SAW filters that provide either a 3.84MHz or 17MHz pass-band response [14].

All signal sources related to RF up/down conversion and the mixed signal interface are derived from the synth board as a common high stability reference. The synth board generates the RF local oscillator, IF local oscillator and ADC/DAC sample clock signals necessary to support a 4-channel MIMO transceiver.

C. VHDL Code Architecture

Figure 3 shows the VHDL code architecture inside the FPGA [14]. The VHDL software blocks fall into two categories: the core signal processing block and the interfacing blocks. The core signal processing block is developed to deal with low-level, high speed and parallel baseband signals, though it remains an open issue regarding the digital processing partitioning between FPGA and DSP. The interfacing blocks are designed to interface other components on the platform, and because FPGA has accesses to almost all other configurable components, the ARM is able to control and configure the whole platform simply by reading or writing corresponding control registers embedded in the FPGA interfacing blocks.

III. Implementation Methods And Limitations

The concept of "Hardware in a Loop" has been

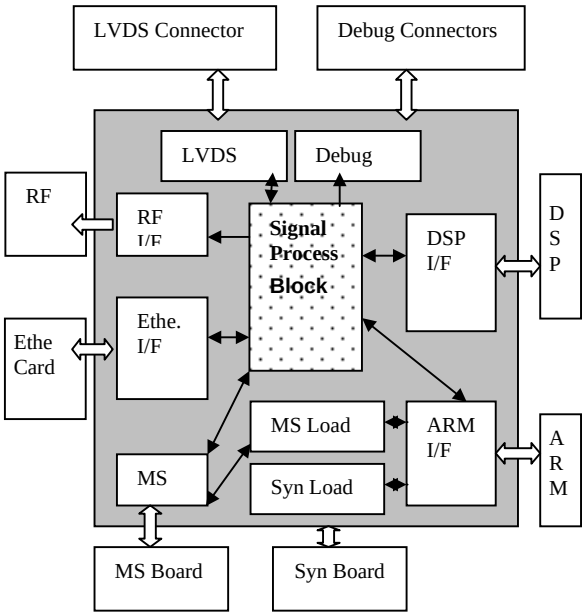

Figure 3. VHDL Code Architecture

addressed in [15] to develop a flexible rapid prototyping platform. The first step is to transmit simulated signals over the air interface, to receive them and to feed them back to a simulation environment. Also referred as off-line processing, this provides a flexible and efficient way to evaluate algorithms facing the problems of a real world propagation channel. Hence, improved physical layer algorithms are moved onto the hardware, resulting in a hybrid system in which the signal processing is partitioned between real time platforms and off-line PCs. Finally, a full working prototype can be achieved as a result of this smooth evolution.

Powered by its flexible architecture, the MIMO testbed can be implemented in either completely real time or offline modes, providing a possible smooth evolution between them. Research capabilities under these two extreme cases will be analysed in the following paragraphs to shed light on the operational capability of the MIMO testbed and associated algorithms.

A. Off-line Implementation and Limitations

In a completely offline implementation, the platform receiver directly forwards the data generated by the ADCs to user's PC. Then, all the digital signal processing functions, including digital IF demodulation and baseband signal processing, are executed in a PC-based simulation environment. This method evaluates the system performance over the real channels while taking advantages of powerful simulation tools. Also, by introducing fixed point processing in PCs, the final result has little bias compared with real time systems. High efficiency, high flexibility and reasonable accuracy feature the offline implementation and it has been widely used in channel measurement and early testing campaigns.

However, running at a rate of 60 Msamples per second and 12bits per sample, each single ADC generates a data stream with a bit rate of up to 720Mbit/s. The data needs to be stored in on-platform-memory or simultaneously forwarded to the PC through a high bandwidth interface. In narrow band implementation, decimation can be applied after ADCs to reduce the equivalent throughput. In the current configuration, offline implementations are limited by the maximum 2MB buffer inside FPGA and the 10Mbit/s Ethernet bandwidth between the platform and PC server.

Assuming a MIMO channel measurement campaign using the same principle as described in [3], where near-orthogonal PN sequences are transmitted simultaneously and then captured and stored at the receiver for further processing to extract the channel matrix. Then we obtain the following equations which describes the measurement limitations caused by the platform output bandwidth:

$$N = \frac{BW}{P \times L \times Q \times S} \qquad R = \frac{BW}{P \times Q \times S} \qquad R = N \times L$$

N: Number of MIMO channel matrix estimates per second (channel update frequency)
BW: Platform output bandwidth (Data acquisition bandwidth / Platform throughput)
P: Numbers of receive antennas (Parallel ADC channels)
L: Length of training PN sequence
Q: Quantization bits per sample (fixed 12bit/sample in the MIMO testbed)
S: Over-sample rate (samples per symbol)
C: Chip rate of training PN sequence.

In a typical configuration where BW=5Mbit/s, P=4, L=200, Q=12bit/sample and S=20 samples/chip, we obtain N=26 and R=5200 chip/s. We can see from these equations and figures that the chip rate R, which also represents half the channel bandwidth under measured, is bounded by almost fixed parameters (BW, P, R). Thus given any reasonable S, the offline implementation is limited for narrowband channel measurement with a bandwidth below 80kHz. On the other hand, the N value suggest that given a reasonable value of L which allows us to introduce enough orthogonality among different PN sequences to validate the channel estimation algorithms, the channel update frequency 'N' with a typical value of 26 is just sufficient for indoor MIMO channels where the Doppler frequency is relatively low [3].

However, the platform does provide two possible upgrades. One is to directly connect the FPGA with an extra high-speed memory board using the serial LVDS data interface. The LVDS interface supports a bandwidth up to 240Mbit/s bi-directional, allowing the offline measurement of a channel with a maximum bandwidth of about 4MHz and an update rate of about 1000times/s. Taking the 16Mbptes SDRAM, which is originally used as ARM's

external memory, as a temporal buffer to store data is another possible upgrade solution.

B. Real Time Implementation and Limitations

A real time implementation is able to bring more MIMO issues into consideration for validation such as: transceiver architecture, software-hardware partitioning, real time processing efficiency and capability, hardware area optimization, packet structure and coding, feedback and cooperative communications, etc. Compared to offline implementation, the limitation of a fully real time system mainly comes from the available digital processing resources, namely, the computational capability provided by on-board FPGA and DSP.

The limitations of real time implementation can be considered by comparing the available computational capability with the computational requirements of certain MIMO decoding algorithms. The on-board DSP is able to provide a capability of up to 4,800MMACs of 16-bit width [16]. The performance of the FPGA, which depends on the area optimization, is much more difficult to evaluate. However, the FPGA provides 80 9-bit-wide dedicated multipliers, plus other of up to 100 9-bit-wide traditional multipliers constructed with logical elements [17-18], achieving an upper bound of 180 9-bit-wide hard multipliers available. Driven by a 120MHz clock, the computational capability bound of the FPGA is estimated as 21,600MMACs. Thus each platform provides a total capability of 26,400 MMACs consisting of 9-bit-wide multipliers.

Consider the implementation of Alamouti's space-time block code [19] in an indoor environment, where the channel is updated in a relatively low rate. The computational load caused by channel estimation could be neglected. From [19], we find that $2N^3$ MACs are needed in the combiner and other $2\times N\times M$ MACs in the maximum likelihood decoder during the decoding phase of each space-time symbol. Here, N denotes an NxN antenna array and M is for M-PSK modulation order. Thus given a symbol rate of R, $2\times R\times(M+N^2)$ MACs per second are needed for real time decoding. In a typical configuration with M=4 (QPSK) and N=4, R can then be calculated as bounded by 660M symbol/s. This is of course an un-achievable upper bound based on many assumptions we have had to make. However, the estimated result suggests that the MIMO platform will have sufficient processing resources for a typical real time MIMO implementation for indoor channels.

IV. Current Developments

A Narrowband (3.84MHz) off-line BPSK single antenna system has been tested by storing sampled data in a short timing window (0.5ms, 30K samples) and demodulating the receive data in Matlab, using both coherent and non-coherent methods. The problem of digital synchronization has been investigated. Two simple algorithms for frequency offset estimation and coherent demodulation, and three other simple algorithms for non-coherent demodulation have been developed and compared in Matlab. A novel non-coherent demodulation algorithm was then chosen to further develop into a prototype using VHDL programming. The gate level simulation turns out to be successful, and the demodulation block is now being integrated into the whole system for real time testing. Subsequent work is to develop a wideband (up to 17MHz) BPSK real time single antenna system and to extend both systems to accommodate MIMO antenna configurations.

V. Conclusions And Future Works

This paper reviews the architecture and capability of the MIMO testbed recently set up at King's College London. We firstly presented the system architectures at different layers. This provides the flexibility to be configured into either a real time, offline, or hybrid research prototype. Then we investigated the system capabilities in real time and offline implementations and find that, because of the powerful on-board processing resources and insufficient data acquisition interface bandwidth, the MIMO testbed is most suited for real time research. We also provided two possible upgrade solutions to increase the output bandwidth of the off-line system, and suggest a development methodology to gradually evolve from off-line to real time.

Future work aims to bring real time feedback-back based signaling schemes in particular into consideration, which off-line system implementation will not allow.

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